Centre for Wireless Communications

Model-based Exploration of the Design Space for Heterogeneous Systems on Chip

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presentation for WSA course by Marika Moilanen
Outline

- Introduction
- Design flow for heterogeneous architectures
  - The proposed method
- Architecture blocks
- Results
- Example for a heterogeneous processor/FPGA based architecture
- Conclusions
Introduction

- The goal of the paper: To provide estimations of implementations specific parameters (throughput, power dissipation, silicon area) by means of cost function

- Computational demands are higher than the performance of today's programmable processor based platforms

- Different forms of flexibility is required:
  - Short innovation cycles
  - Adaptation to standard updates
  - Runtime adaptation

- Dedicated hardware implementations offer better throughput and power dissipation but flexibility is worse

1.6.2005
High performance SoC (Systems on Chip) has to include different architecture blocks to provide the required performance and to ensure sufficient flexibility.
Introduction

- Systems have to be partitioned into system blocks and mapped to appropriate architecture blocks

- To explore the available design space in an early phase of the design process gives better results in implementing a SoC
Design flow for heterogeneous architectures

- Feedback loops consume much time
  - Arise when the specifications cannot be met with the first approach

- Some alternatives at system level
  - Initial partitioning/mapping has to be changed (feedback from architecture level to system level)
  - To restrict the parameters of the design -> loss in system quality but reduced redesign time and effort
Design flow for heterogeneous architectures

- Several approaches have been proposed to solve this design space exploration problem
  - All of these try to integrate several design tools into the design flow
  - Problems include interfaces of different tools

- A model-based partitioning strategy for efficient design space exploration is proposed
  - In an early stage of the SoC design, the design space exploration is required
  - Partitioning/mapping should be done with important features in mind (power dissipation, silicon area, throughput...)
  - A system designer needs deeper hardware/architecture knowledge

- A cost evaluation tool supports the system designer
  - Requires information about specifications
  - Access to a model library
Design flow for heterogeneous architectures

- Non-realistic partitionings/mappings avoided in early phase
- A need for several models and large model library

1.6.2005
Architecture blocks

- Basic operations have to be implemented on architecture blocks available for SoC architectures
  - Cost function $C = A \cdot T \cdot E_{\text{per sample}}$ parameters can be found
  - $A =$ silicon area
  - $T =$ sample time
  - $E_{\text{per sample}} =$ energy to compute one output sample
- Models of basic operations were first studied from existing discrete components
  - Cost ratio expected can be found although considered processors and FPGAs are not available for core components
  - In future, test implementations to on-chip macros for SoC architectures
Results

- Dependency of the cost on implementation specific parameters

- To get fairly accurate models for different architecture blocks a optimization is needed according to the specific architectural features of a block

- In DSP implementations the critical path and power dissipation was examined and optimized
Results

- While examining power dissipation it was noticed that the energy per sample is better metric than the power consumption.

- Optimizing FPGA
  - Fixed hardware structure of an FPGA can increase the performance of a design significantly.
  - The considered operations were optimized for the architecture blocks applying optimization strategies from system level down to implementation level.
  - The cost could be decreased by a maximum factor of 17 by optimizing an implementation for a specific architecture block.
Results

- Comparison of implementations on different architecture blocks

Exemplary comparison of normalized ATE-cost ratios
Results

Comparison of cost ratios for programmable processors

- Celeron 733 MHz; Plain C (first inst.)
- TMS320C6711 (first inst.)
- Trimedia (first inst.)

- Celeron 733 MHz; MMX/SSE (first inst.)
- TMS320C6711 (free comp. resources)
- Trimedia (free comp. resources)
Example for a heterogeneous processor/FPGA based architecture

- System may contain several smaller system blocks
  - The implementation alternatives and specific parameters are studied
  - Threshold-based image segmentation
- System based on heterogeneous architecture consisting of an Altera Apex FPGA including a NIOS RISC processor core
  - Soft-core (high flexibility and easy implementation of multi-processor)
  - Processor core can be programmed with C/C++
- Two implementation alternatives was implemented
  1) Pure HW-FPGA (algorithm in a hardware language and then synthesized)
  2) Synthesized logic in cooperation with the processor core
Example for a heterogeneous processor/FPGA based architecture

- Heterogeneous system including the processor core is by one order of magnitude more flexible than pure HW-FPGA

- Specific parameters of the two alternatives for 256*256 pixel image are compared

<table>
<thead>
<tr>
<th>Implementation</th>
<th># logic cells [LEs]</th>
<th># memory bits [ESB bits]</th>
<th>max. freq. [MHz]</th>
<th>time of extrema calc. [cycle]</th>
<th>total time [cycle]</th>
<th>energy per sample [J/sample]</th>
<th>flexibility (e.g. 1/redesign time) [h⁻¹]</th>
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</thead>
<tbody>
<tr>
<td>HW</td>
<td>2127</td>
<td>5120</td>
<td>43</td>
<td>532</td>
<td>132210</td>
<td>1·10⁻¹¹</td>
<td>≈ 0.1</td>
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<tr>
<td>HW/SW</td>
<td>4025</td>
<td>32800</td>
<td>35</td>
<td>11855</td>
<td>143533</td>
<td>2.54·10⁻¹¹</td>
<td>≈ 1</td>
</tr>
</tbody>
</table>

Table 3. Feature comparison of design alternatives for a processor/FPGA based SoC
Conclusions

- Implementation specific parameters for basic operations are needed for exploring the design space for heterogeneous SoC.
- This way the optimal implementation can be chosen.
- A model based design space exploration concept is proposed.
- Cost modelling of the basic operations on different architecture blocks is required.
- Strategy results (implemented on discrete components) have been presented.
- Cost function analyze shows 4 to 7 order of magnitude difference in physically optimized and software based solution in DSP.
- A real example for a heterogeneous system is described.